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# Integration of EMI Shielding Design for Substrate Package Isolation

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***Authors' contributions***

*This work was carried out in collaboration between both authors. Both authors read, reviewed and approved the final manuscript.*

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## ABSTRACT

This paper presents a modified substrate design that would enable a bottom electromagnetic interference (EMI) shielding protection for EMI sensitive integrated unit (IC). The modified substrate design is applied and incorporated to the existing and known shielding technique to fully proof the structure to external interference through the application of EMI shielding layer on the substrate configuration. The EMI shielding layer will be connected to the surface coating (EMI shielding) and ground channel of the substrate and the external board.

*Keywords: EMI; integrated circuit; semiconductor; substrate.*

## 1. INTRODUCTION

Electromagnetic interference (EMI) shielding became known in cellular phone manufacturing to fully proof the system from external disturbances (or interference) that may create damage and/or degrade the functionality of the device. EMI may come from multiple sources but can be categorized as man-made or interference arising from other or neighbor electronic devices, and naturally occurring or interference created naturally by thunderstorms or lightning.

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EMI is present in our environment and cannot be avoided but designer and engineer eliminates the impact of external interference to the electronic devices through different shielding techniques such as integrating metal cans and board-Level shielding that is coupled to the grounding connection of the system. This are conductive metal that envelops the EMI prone area or integrated unit in a system as shown in Fig. 1A.

Continuous drive for miniaturized and thinner version of packaging requires reduced footprint for electronic devices leading a way to explore package level shielding. A package level pre-applied surface coating in Fig. 1B has a conductive material that is deposited in the outer layer of the integrated circuit (IC). The conductive material forms adhesion to the top and sidewall area of the molding compound to cover the silicon die which is vulnerable to interference. On the other hand, compartment shielding in Fig. 1C is applicable for unidirectional interference wherein you can integrate a metal shielding on a single or one side of the unit. this technique is applicable if the source of the interference is known inside the system.

One of the opportunities seen is the vulnerability of the bottom section of the unit which lacks shielding capabilities. Only the top and sidewall section of the unit is covered by the known shielding method wherein the bottom can be a potential entry point for electromagnetic interference. This paper presents a substrate design wherein it can be incorporated to the different shielding method to produce an overall protective structure of EMI shielding for IC. The proposed substrate design focused on a metal conductive layer on the substrate that will be connected to the ground and EMI shielding channel to completely cover the silicon die from external interference or EMI.

## 2. DESIGN METHODOLOGY

Realization of the design improves the conventional package level shielding structure by incorporating an EMI shielding layer on the substrate. The shielding layer protects the bottom area of an integrated unit from interference which is absent on the conventional structure and method of shielding. The 3D illustration of the modified design of substrate is shown in Fig. 2. Note that as the die technology becomes smaller, faster, and thinner, circuit metallization also becomes smaller, thus the device or package in general becomes sensitive and susceptible to EMI. Moreover, it is worth noting that with new and continuous technology trends and breakthroughs, challenges in semiconductor manufacturing are inevitable [1-4].

A metallic layer is incorporated on the top surface of the substrate wherein a silicon die is mounted on top of the EMI shielding layer through non-conductive die attach films. A wire is mounted on the bonding pads and the ground wire connection can be attached to the EMI shielding layer. The clearance between the bonding pad and EMI shielding layer is explained in Fig. 3. A 50 microns distance is required to separate the bonding pads from the EMI shielding layer with a 25 microns tolerance from the etching process. Technically, the anticipated range of the clearance is 25 to 75 microns.

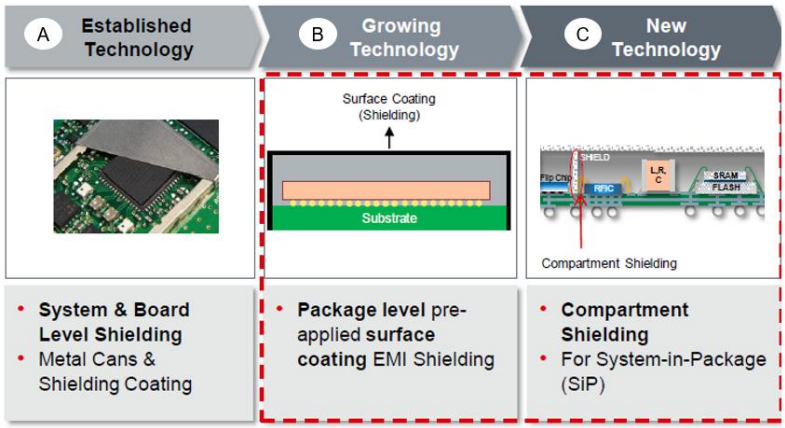


**Fig. 1. EMI shielding techniques**

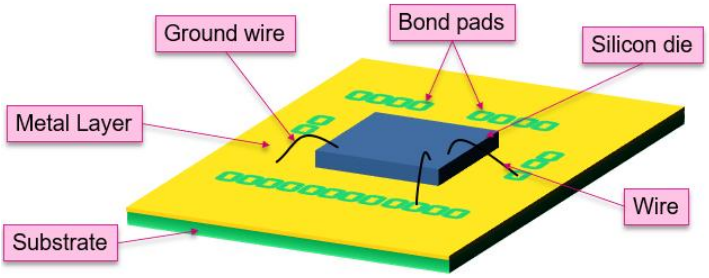


**Fig. 2. Substrate with EMI shielding layer**

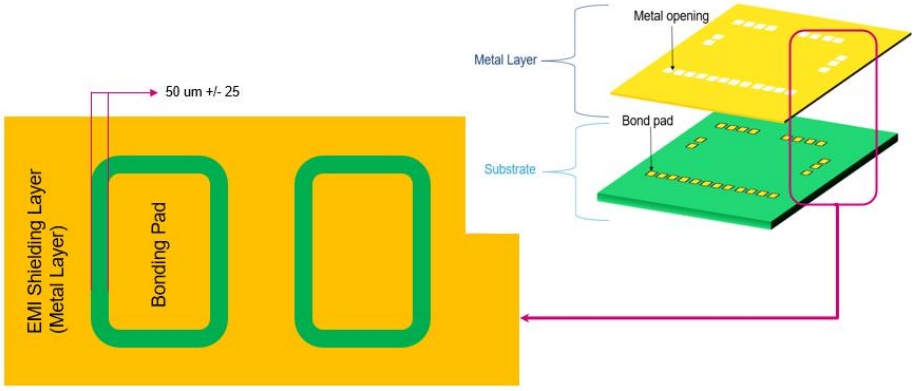


**Fig. 3. EMI shielding layer**

Upon application, the EMI shielding layer will be physically and electrically connected to the surface coating (package level EMI shielding) as illustrated in Fig. 4. The combination of EMI surface coating and the modified substrate design forms a complete isolation of the silicon die to the external interference. Likewise, interference coming from internal source will not escape outside the shielding (applicable power application IC).

To divert the interference, the shielding (surface coating and EMI shielding layer) should be connected to the grounding channel. In the proposed structure, the surface coating has an intermetallic connection to the EMI shieling layer then a grounding connection is established from the EMI shielding layer to the dedicated pin of the substrate. Later, the dedicated pin will be connected to grounding connection of the external board or printed circuit board (PCB). To manufacture a substrate with EMI shielding layer, a copper sheet attach process is required after Nickel-Gold plating (NiAu) is performed on the substrate as shown in Fig. 5.

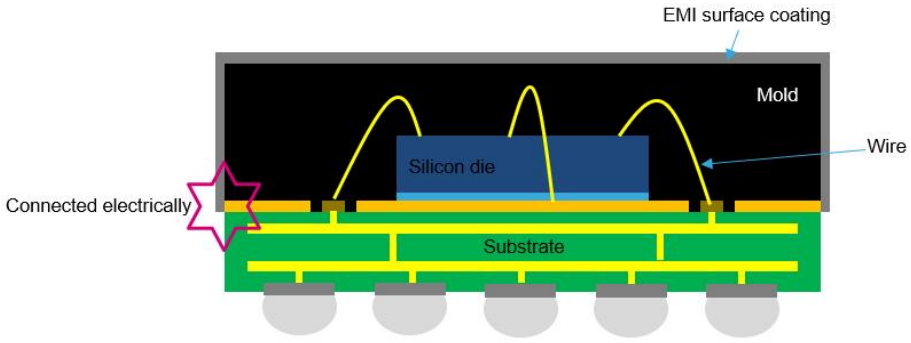


**Fig. 4. Cross-sectional view of the unit using substrate with EMI shielding layer**

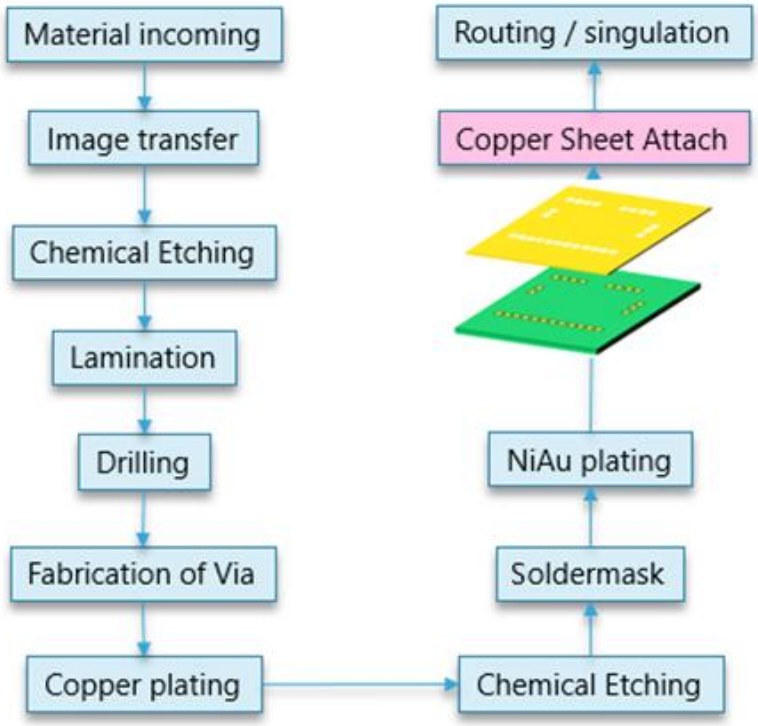


**Fig. 5. Fabrication method**

The copper sheet material is realized through series of: 1) pattern layout generation which defines the design and dimension of the metal opening for the copper sheet; 2) masking process which is the isolation of the define pattern from part of the copper that will be removed; 3) etching process is the removal of the exposed copper through chemical etchant; and 4) selective plating that is required to coat the area where the grounding connection will be attached. Worthy to note that generally, fabrication or process flow varies with the product and the technology [5-9]. Also, important to note that EMI and electrostatic discharge (ESD) share few similar characteristics. Hence, it is imperative that the fabrication method and all other assembly processes observe proper ESD checks and controls. learnings shared in [10-12] are very helpful to realize proper and effective ESD-related controls.

## 3. CONCLUSION AND RECOMMENDATIONS

An improved substrate package design is presented for EMI shielding capability. The limitations from the standard design is eliminated through the new design and the specialized fabrication process of the device. Ultimately, the package design solution would address the EMI issues occurring on sensitive and complex designs.

Though the paper is focused on the EMI shielding ability, continuous process and design improvement is imperative to foster and sustain high quality performance of semiconductor products and its assembly manufacturing. Prototypes are helpful for future works to validate the effectiveness of the improved substrate device with integrated EMI shielding design, with necessary simulation results and hardware results.

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## COMPETING INTERESTS

Authors have declared that no competing interests exist.

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